Sr. No.	Name of Staff Member	Title of Paper	National Paper	International Paper	Venue and Date
1	Prof.Sandeep Tiwari	Application Of Artificial Intelligence in Bioinformatics/Life Science		01	Raipur , January 2013
2	Prof. Rahul langde	PID Controller for Ball and Beam System		01	
3	Prof. Rahul langde	Second Order Twisting Sliding Mode Control of Multi-agent Network with Input Disturbance		01	IEEE international conference at Chennai
4	Prof. Rahul langde	GSM and GPS based Real Time Vehicle Positioning System		01	
5	Prof. Rahul langde	Energy Meter Billing System with Prepaid and Postpaid Facility		01	
6	Prof.Sandeep Tiwari	Bit Error Rate Determination for Digital Audio Broadcasting Using Different Modulation Scheme		01	June 2014
7	Prof.Ishan Patil	Enhancement of imagery in poor visibility conditions.		01	
8	Prof.Avinash Ikhar	Enhancement of Blood Vessel for Microaneurysm Detection and Diabetic Retinopathy using an Ensemble Based System		01	
9	Prof.Firz Akhtar	Design of home automation on xilinx using VHDL		01	Nagpur, 8th & 9th Jan 2014
10	Prof.Firz Akhtar	Design and implementation of smart home automation system on FPGA		01	3rd June 2014
11	Prof.Firz Akhtar	GSM Communication using FPGA for implementating home automation system		01	12th and 13th April 2014

12	Prof.Firz Akhtar	Performnce of FPGA for Home automation using VHDL		01	7th July 2014
13	Prof.Ishan Patil	FLOATING POINT BASED UNIVERSAL FUSED ADD-SUBTRACT UNIT		01	DOI: 10.1007/978-81-322-1602-5_29, © Springer India 2014
14	Prof.Ishan Patil	FPGA Implementation of USB 2.0 Protocol.		01	Feb 2015
15	Prof.Ishan Patil	Implementation of Floating Point Fused Basic Arithmetic Module Using Verilog		01	Tamilnadu , 2nd , 3rd & 4th April 2015 DOI:10.1109/ICCSP.2015.7322647 © IEEE 2015
16	Prof.Nilesh Mohota	FPGA implementation of 2D DCT Architecture for JPEG		01	Feb 2015
17	Prof.Nilesh Mohota	An efficient implementation of MIMO OFDN Transreceiver on FPGA		01	June 2015
18	Prof.Tushar S.Muratkar	An area optimized, Low latency, High Throughput Pipelined Doube precision Floating point Multiplier using VHDL on FPGA		01	Nagpur, 8th & 9th Jan 2014